Table 1 – vLCD\_CLEAR\_TOP Logic Test Plan

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Test Writer:** | | Steven Zehner |  |  |  |  |
| **Test Case Name:** | | LCD Clear Top Logic | **Test ID #:** |  |  | Clear Top Logic Test 1 |
| **Description:** | | Verify operation of the vLCD\_CLEAR\_TOP function with Logic Analyzer | **Type:** | |  | White Box |
| **X** | Black Box |
| **Tester Information** | |  |  |  |  |  |
| **Name of Tester:** | |  | Date: |  |  |  |
| **Hardware Ver:** | | 1.0 | Time: |  |  |  |
| **Setup:** | Connect STK600 Port\_K\_ to the Logic Analyzer. A task is created that calls the vLCD\_CLEAR\_TOP() function. | | | | | |
| **Test** | **(Test Variable)** | **Expected Result** | **Pass** | **Fail** | **N/A** | **Comments** |
| 1 | Return Home | Logic Analyzer Shows 0b00000010 |  |  |  |  |
| 2 | Write Spaces | Logic Analyzer Shows 0b00100000 |  |  |  |  |
| 3 | Return Home | Logic Analyzer Shows 0b00000010 |  |  |  |  |
| **Overall Test Result:** | |  |  |  |  |  |